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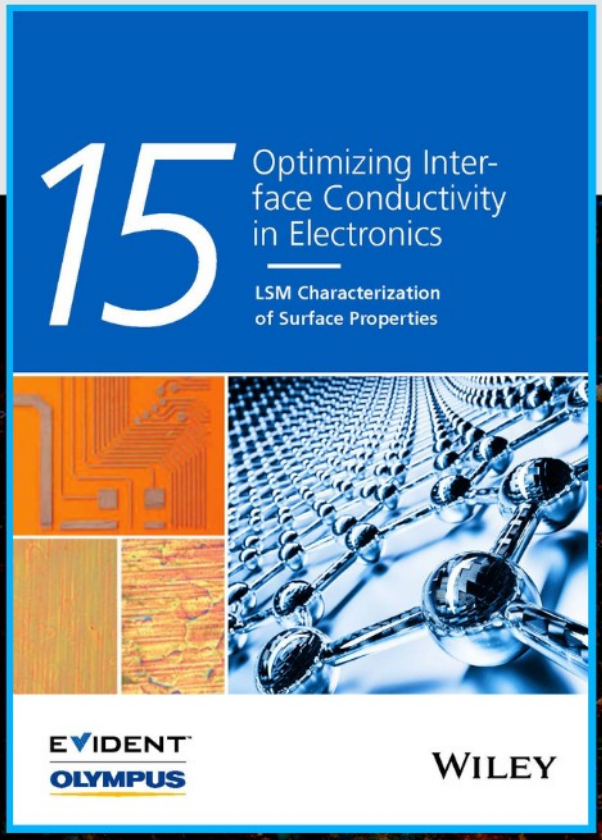
# Optimizing Interface Conductivity in Electronics

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# Scalable Microfabrication of Folded Parylene-Based Conductors for Stretchable Electronics

*Florian Hartmann, Marie Jakešová, Guoyong Mao, Marta Nikić, Martin Kaltenbrunner,* Vedran Đerek,* and Eric Daniel Głowacki**

**Electronics implemented on biocompatible ultrathin substrates like polyethylene terephthalate, polyimide, or parylene enabled a wide range of conformable, lightweight smart wearables and implantables. However, applications in such dynamic environments require robust devices that adjust and stretch while maintaining their functionality. Universal approaches that unite scalable, low-cost fabrication with high performance and versatile, space-efficient design are sparse. Here, stretchable architectures of parylene enabled by Origami-inspired folds at the micrometer scale are demonstrated. Parylene is directly deposited onto anisotropically etched silicon molds to greatly reduce bending stress, allowing folds with bending radii of a few micrometers. 50-nm-thick gold conductors fabricated on the folded parylene facilitate electronics with a stretchability of up to 55% tensile strain. The conductors sustain a resistance below 20 Ω during reversible stretching of more than 10 000 cycles, enabling long-term operation in practical settings. This method presents a versatile tool for the microfabrication of stretchable devices with tunable properties.**

## 1. Introduction

Embodiments of stretchable electronics enable a wide range of applications from implantable (bio-) electronics,[1] autonomous wearable devices,[2] to electronic skins for soft robotics.[3] The transformation from rigid to flexible and ultimately stretchable devices is typically achieved by utilizing intrinsically stretchable materials or through structure-enabled (rigid-island) designs. Intrinsically stretchable materials such as liquid metals,[4] elastic composites,[5–7] or (semi) conducting polymers[8,9] are highly stretchable, albeit often at the expense of significantly lower conductivity compared to their (cost-intensive) bulk ingredients, and inherently exhibit strain-dependent properties. Structure-enabled designs benefit from established non-stretchable materials with high performance, which gain macroscopic stretchability through structural deformation such as out-of-plane buckling, bending, or twisting.[10] Those concepts are often based on serpentine-shaped conductors[11] that connect rigid islands that host complex electronic devices or chips.[12,13] While this approach allows a high degree of miniaturization through microfabrication, serpentine-shaped interconnects usually consume the majority of the device area, hampering efficient use of available space. Mesh-type electronics based on Kirigami-structures suffer from similar problems yet excel with high stretchability and simple fabrication processes.[14] These advantages render Kirigami-structures a promising solution as conformable electrodes for auditory brainstem implants[15] or highly stretchable strain sensors.[16] However, higher stretchability is often only achieved by introducing complex cutting patterns and with a general increase of the conductor resistance. Stretchable electronics based on wrinkling of

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ultrathin materials[17,18] (1-µm thickness) allow for high device density but necessitate pre-stretched elastic substrates, which reduces applicability. This is also the case for rigid island designs with buckled interconnects.[19,20] Additionally, both concepts suffer from high internal stress in the relaxed state.

To overcome these limitations, fabrication solutions that allow engineered folding of substrate and electronics could allow tunable stretchability while simultaneously providing a high device density. In contrast to Kirigami, Origami approaches—the Japanese art of folding—are rarely used in stretchable electronics. Existing demonstrations mainly utilize folding patterns to acquire static 3D-objects out of 2D electronic devices and materials.[21–25] However, folded devices that are used in dynamic environments would benefit from controlled, built-in fold mechanisms that result in high stretch ratios.[26] Introducing a multitude of folds is challenging, as post-fabrication folding introduces high mechanical stress and only allows a few folds per centimeter (<10 $cm^{-1}$) due to limitations in available techniques.[27–29] State-of-the-art applications, such as implantable electronics or imperceptible wearable devices, require scalable fabrication tools for structures with hundreds of folds that cause little stress on the electronics itself.

Here, we present Origami-based concepts, detailed design rules, and fabrication methods for stretchable electronics on microfolded parylene substrates. The folded substrates are produced using standard microfabrication tools and processes, which allows for scaling of devices and engineered structure properties. We use anisotropically-etched silicon to produce molds with V-shaped grooves for the deposition of parylene-C. Encapsulated gold conductors form ultrathin (4-µm total thickness) stretchable electronics enabled by the accordion-type structure of the microfolded parylene-substrate. The conductors feature up to 267 folds per cm and achieve a stretchability of up to 55% tensile strain (from their stress-free state), whereby the stretchability is tuned by the spacing-to-groove ratio. Repeated stretching to 20% strain shows only a small increase of the resistance, independent of design and scaling, even after more than $10^4$ cycles. With this concept, we demonstrate a new approach to fabricate biocompatible stretchable electronics with tunable properties and high performance.

## 2. Results and Discussion

Stretchable electronics based on folded structures are usually achieved using thin flexible films, such as polymers or nanocellulose paper, and introducing folds after the fabrication of the devices. This, however, exerts high mechanical stress when folds are formed and—in case of wrinkling or buckling—additionally requires pre-stretched elastomers as an underlying substrate. Instead, we here developed a fabrication strategy that enables microfolded structures to be created in the substrate directly. Our method is based on the deposition of the polymer parylene-C onto 3D structured silicon molds, which allow wafer-scale microfabrication of folded substrates and electronics. Parylene-C has emerged as a leading material for microfabricated biomedical devices and neural interfaces, due to its excellent dielectric properties, biocompatibility, and suitability for microfabrication techniques.[1,16,30,31] In contrast to other polymers such as polyethylene terephthalate (PET) or polyimide, parylene (and its derivatives) is deposited through chemical vapor deposition (CVD), which allows homogeneous and conformal coverage of 3D objects at room temperature. Depositing parylene-C on grooved molds directly produces films with built-in folds. The folds persist in the film's relaxed state and allow both stretching and compressing of the films (**Figure 1**a). Etching of silicon enables high precision molds with V-shaped grooves in the micrometer scale. Parylene films deposited on such molds feature hundreds of folds per centimeter, with a total structure height of 55 µm (which is thinner than the thickness of regular

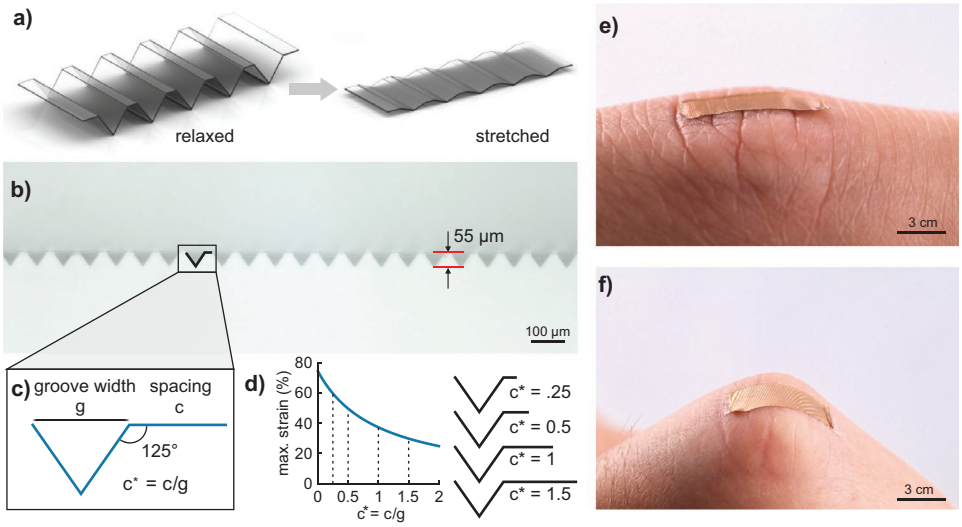


**Figure 1.** Microfolds-enabled stretchable structures. a) Schematic of a folded parylene film in relaxed (left) and stretched (right) state. b) Optical image of an unstretched and unsupported film with microfolds. The total height of the structures is about 55 µm. c) The design of a single repeating unit is governed by its groove width *g* and spacing width *c*. d) The spacing-to-groove ratio *c** determines the maximum stretchability that is achieved through unfolding the structures. e) Thin and lightweight parylene films are imperceptible on a human finger and f) allow stretch ratios similar to those of skin.

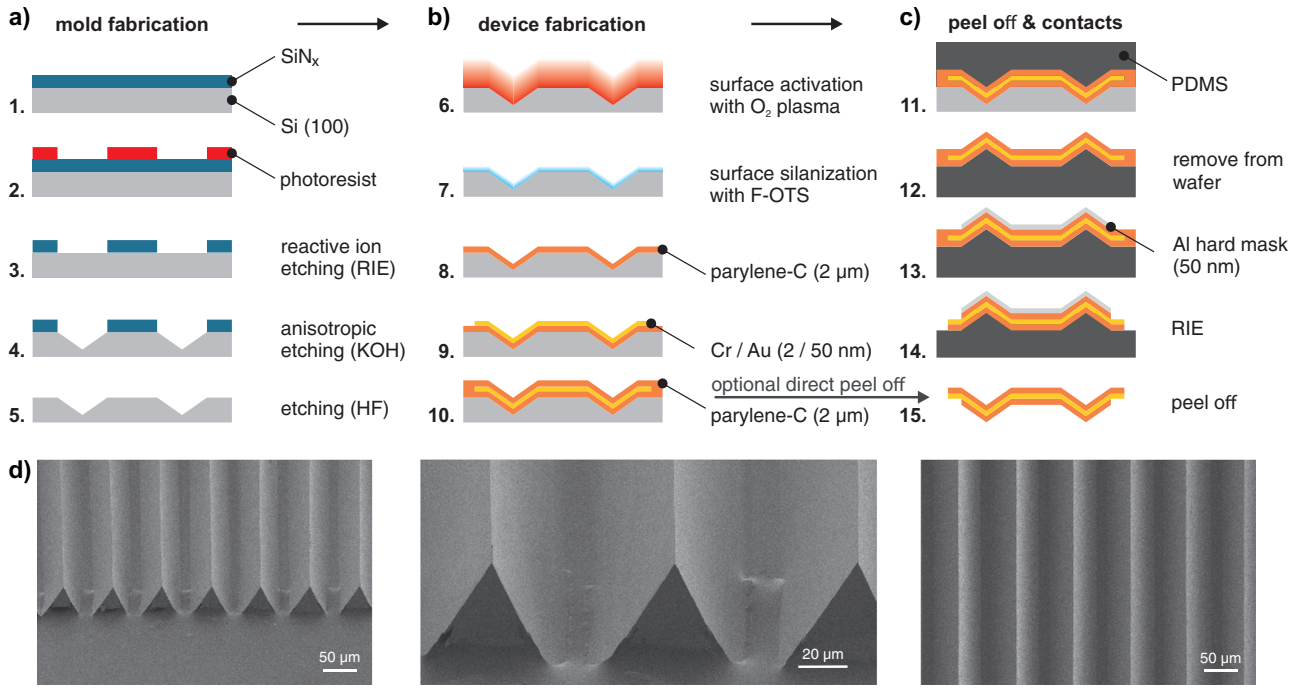


**Figure 2.** Fabrication of microfolded parylene films. a) Mold fabrication requires anisotropic etching of silicon (100) patterned with silicon nitride ($SiN_x$). b) Thin foils of parylene-C are obtained by CVD on the molds, to form the substrate and encapsulation of electronic layers. c) A PDMS support eases peel-off and serves as a carrier for additional patterning and device fabrication. d) SEM images of folded parylene films. The sharp and regular features of the mold allow for folds in the micrometer scale.

80 g $m^{-2}$ copy paper) (Figure 1b, Figure S1, Supporting Information). The fold-pattern is inherent to the etched silicon itself; anisotropic etching of silicon (100) allows scalable fabrication of pyramidic or grooved molds in case of square or rectangular shaped etch-masks, respectively. The angle between the flank of the groove and the surface measures 125°, and is fixed due to the crystal structure of silicon (Figure 1c). The groove width $g$ and the spacing $c$ between two grooves can be freely adjusted by the design of the etch mask and are mainly limited by the precision of available microfabrication tools. Adjusting the spacing-to-groove ratio $c^* = c/g$ determines the maximum stretchability that is achieved through unfolding of the structures with respect to their relaxed (as-fabricated) state (Figure 1d, Table S1, Supporting Information). This geometric-limit is thus given by

$$\varepsilon_{\max}(c^*) = \frac{\sin^{-1}(35°) - 1}{c^* + 1} \quad (1)$$

While the spacings between grooves can be used as rigid islands for active electronics such as sensors or light-emitting-diodes and allow high device density, the grooves function as stretchable interconnects. As a proof-of-concept, we here demonstrate stretchable gold-metal conductors fabricated on parylene stripes with hundreds of folds and investigate the influence of different $c^*$ ratios and dimensional scaling on their stretchability. With a $c^*$ ratio of ⅓, the structures reach a maximum tensile strain of 55%, which is higher than extensions that occur on our skin, and makes this concept a good choice for wearable applications or systems that operate in dynamic environments (Figure 1e,f, Movie S1, Supporting Information).

The fabrication of the stretchable conductors is split into mold fabrication, device fabrication, patterning, and peel-off. For the molds, silicon (100) wafers are anisotropically etched in potassium hydroxide (KOH, 30%), utilizing patterned silicon nitride ($SiN_x$) as an etch mask (**Figure 2**a). To this end, $SiN_x$ is deposited on silicon and patterned via photolithography and reactive ion etching (RIE). The photoresist acts as an RIE etch mask, which is later removed in acetone or resist remover. The grooved mold is formed by etching the patterned silicon in KOH at a rate of 60–70 µm $h^{-1}$. The stretchable conductors are then directly fabricated on these molds (Figure 2b). However, the silicon surface first requires treatment to reduce adhesion and allow for peel-off in the last step. We found that conventional anti-adhesion coatings based on lab-grade detergents like micro-90 always left residues in the resulting microgrooves. To provide a residue-free anti-adhesion coating, we functionalized the silicon mold via a vapor-phase monolayer treatment with fluorinated silane prior to the deposition of the first parylene-C (2 µm) layer. The gold conductors (50-nm-thick) themselves are deposited through a shadow-mask, resulting in 10 mm × 4 mm size stretchable conductors with 5-mm-long flaps serving as contacts on each side (Figures S2 and S3, Supporting Information). An encapsulating layer of parylene-C (2 µm) places the gold layer into the mechanical neutral plane, reducing stress during mechanical deformation. The parylene films can be directly peeled off from the wafer, or first be transferred to an elastic support layer. To accomplish the latter, the parylene is coated with a thin layer of polydimethylsiloxane (PDMS) and peeled from the silicon wafer. The individual conductors are patterned on the PDMS using RIE to expose electrical contacts

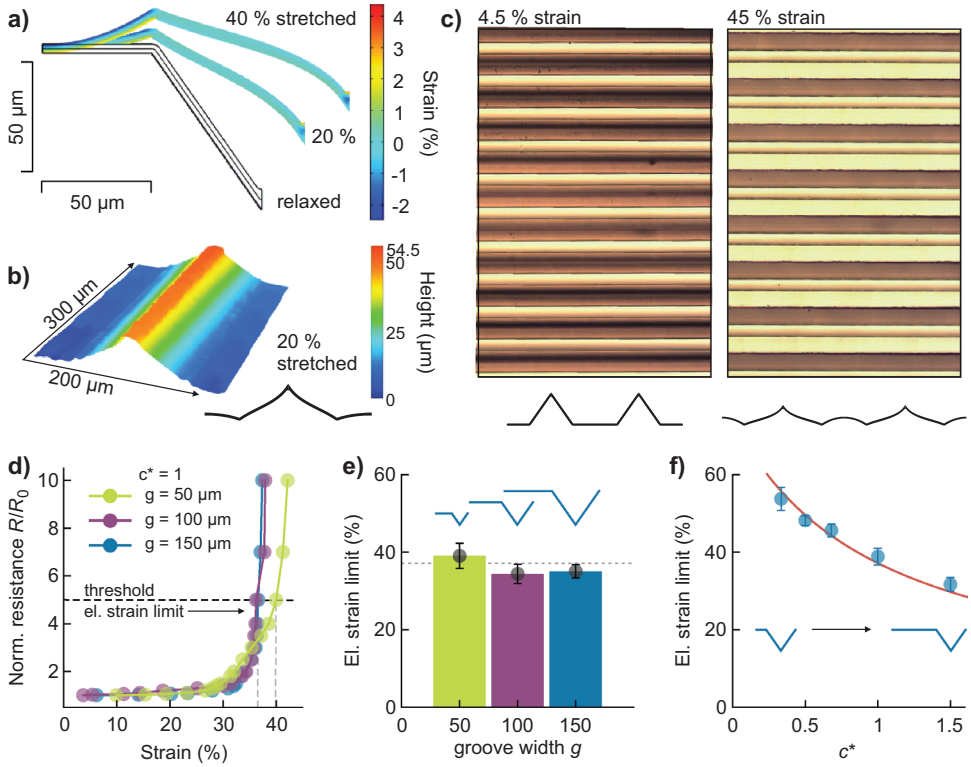


**Figure 3.** Stretchability of conductors. a) FE analysis of micro-folded parylene shows low strain distributions when stretched to 20 and 40%. Strains around folds are greatly reduced as the angles only slightly change during unfolding of the structures. b) 3D optical profile of stretched parylene grooves. c) Optical micrograph of nearly unstretched and stretched structures, and comparison to the model. d) Resistance of stretchable conductors only slightly changes for moderate strains and surpasses the threshold of $R/R_0 = 5$ at the electrical strain limit. Data points represent an average of $n = 3$ samples each. e) Microfolds with 50, 100, and 150 µm groove width are invariant to scaling and all reach an electrical strain limit close to the geometric limit (dashed line). Error bars, standard deviation ($n = 5$). f) Changes in the spacing-to-groove ratio $c^*$ allow engineering of the stretchability and electrical strain limit. The solid red line represents the geometric limit. Error bars, standard deviation ($n = 7$).

and to remove excess material (Figure 2c). Due to the CVD of parylene-C, which is a vacuum process, the pattern of the mold is conformally replicated by the polymer (Figure 2d), exhibiting sharply folded polymer films.

During stretching the resulting strains within the films are low, as evidenced by finite element (FE) analysis (**Figure 3**a, Figure S4, Supporting Information). A conductor ($c^* = 0.5$) stretched to 40% strain receives less than 4% tensile strain and less than 2% compressive strain, whereby the load on the gold film is largest at the tip of the groove. Optical recordings of the height profile qualitatively agree to the FE model, resulting in a height of about 54.5 µm when stretched to 20% (vs simulated height, 53 µm); however, we note that the tip could not be precisely resolved by the microscope (Figure 3b). A comparison of optical images of nearly unstretched (4.5% strain) and 45% stretched conductors (geometric limit for $c^* = 0.5$ is at 50% strain) relates to the FE predicted shapes (Figure 3c,d). The folds at the tips and spacings maintain the folding angle even at high stretches. We investigate the electrical performance of the conductors in terms of relative resistance increase under extension for conductors with an initial groove width of $g = 50$, 100, and 150 µm and various $c^*$ ratios. For this purpose, we use conductors supported by PDMS to ease the handling of samples (Movie S2, Supporting Information). The electrical resistance of the samples remains nearly unchanged until 30% strain but sharply increases close to the geometric limit (Figure 3e). The threshold at which the conductors fail is here defined as a fivefold increase of the initial resistance and the strain that is achieved at this threshold is termed electrical strain limit. With an initial resistance of 14 Ω the threshold is given at >70 Ω (Figure S5, Supporting Information). Comparing conductors with differently scaled folds shows no distinct difference due to scaling (Figure 3f). All three designs achieve electrical strain limits close to the geometric limit, which is readily adjusted by changing the spacing-to-groove ratio $c^*$ as governed by Equation (1). The electrical strain limit of conductors with $c^*$ ratios ranging from 0.33 to 1.5 follows the predicted trend, demonstrating tunable device properties (Figure 3g). Some samples even achieve electrical strain limits above the geometric limit, which is due to the intrinsic stretchability (≈10% strain at break) of parylene itself (Figure S6, Supporting Information). Similarly, gold endures deformation of a few percent strain due to the formation of a crack network.[32] We note that fully extending the stretchable conductors leads to plastic deformation from which they cannot recover their folded shape.

In practical applications such as on-skin wearables or implants, stretchable electronics are exposed to moderate stretches (typically below 30% for human skin).[33,34] We therefore systematically test the resistance increase of the conductors for over $10^4$ repeated stretch-release cycles to 20% strain

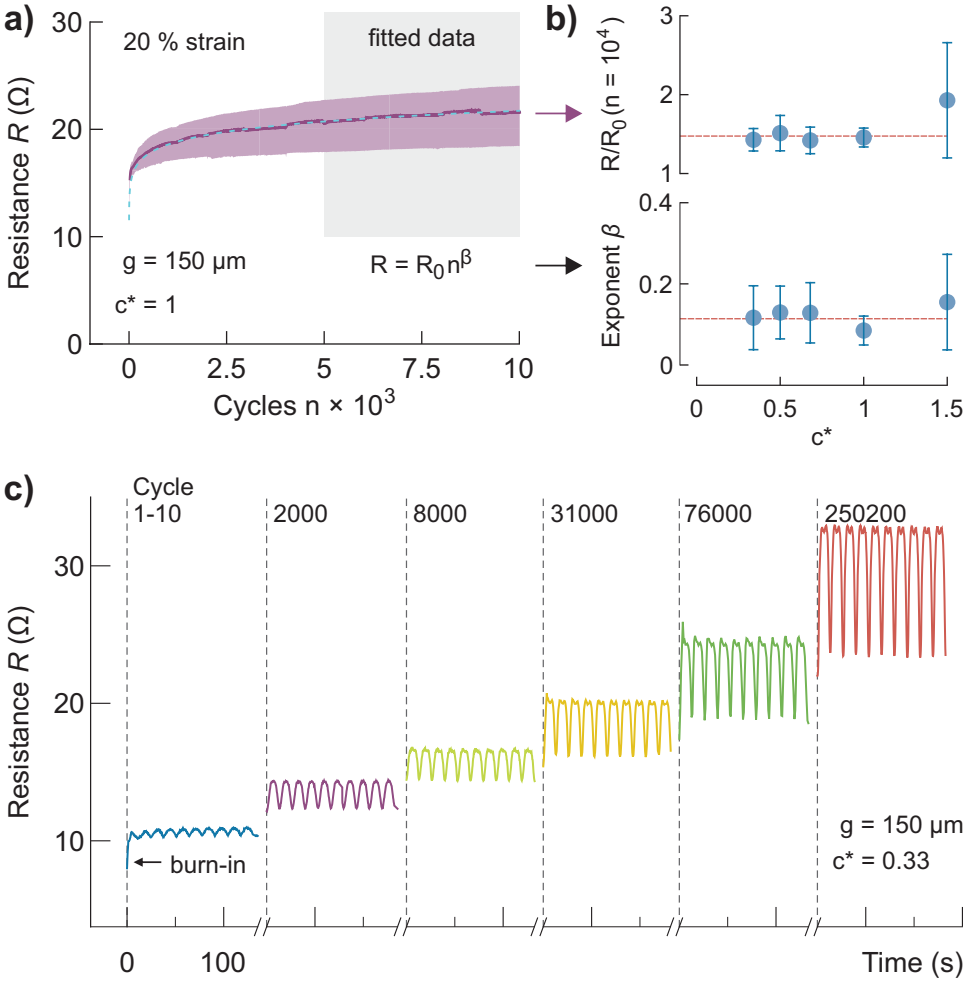


**Figure 4.** Fatigue under cyclic loading. a) Resistance of repeatedly stretched conductors stays low even after $10^4$ stretching cycles to 20% strain. The last 5000 cycles are fitted with a power function (dashed cyan line, exponent beta serves as a fit parameter) to investigate the resistance increase. Data envelope, minimal, and maximal resistance. b) The normalized resistance after $10^4$ stretching cycles stays low (weighted mean = 1.47, dashed line) due to an equally low exponent beta (weighted mean = 0.11, dashed line), independent of $c^*$. Error bars, standard deviation ($n = 8$). c) Conductors feature an initial resistance increase (burn-in) and show a strain-dependent resistance response. Resistance increases to about 30 Ω after $25 \times 10^4$ consecutive stretching cycles to 20% strain.

(a comparison to other stretchable conductor concepts is given in Table S2, Supporting Information). Typically, the resistance $R$ increases most within the first thousand stretch cycles and exhibits small changes afterward (**Figure 4**a). This behavior is typical for crack-induced failure mechanisms and can be described by a power law $R = R_0\, n^{\beta}$. Where $R_0$ is the initial resistance, $n$ the number of cycles, and $\beta$ the exponent, which is a measure of how much the resistance increases per decade. The exponent is obtained by fitting the last 5000 stretch cycles with the power law to better estimate the behavior at large cycle numbers. In addition, the relative resistance at $10^4$ cycles measures the practicability of our approach independent of a model (Figure 4b). Almost independent of the tested conductor geometry ($c^*$ ratios from 0.33 to 1.5), this value stays low with a weighted mean of 1.47. With an initial resistance of 14 Ω the resistance on average increases to 20.6 Ω after $10^4$ cycles. This small rise in resistance results from an equally small exponent of 0.11 (weighted mean), nearly independent of the $c^*$ ratio. The conductors are suitable even for applications that require hundreds of thousand stretch cycles. The resistance of conductors stretched to over $25 \times 10^4$ cycles increases to about 30 Ω (Figure 4c). The strain-dependent resistance increase during a cycle changes from 0.03 to 0.46 Ω per percent strain after $25 \times 10^4$ cycles. This behavior can be explained by a growing number of cracks in the gold film and delamination (Figure S7, Supporting Information). We however note that the highest load acts in the region where the conductors are clamped into the test machine and are therefore inherent to our test setup. The resistance changes in real applications can be substantially smaller.

## 3. Conclusion

In summary, we report a new fabrication technique for stretchable conductors with high performance and low fatigue during

repeated deformation. Our approach is based on the deposition of parylene-C on micro-structured silicon molds. The scalable fabrication process produces microfolded parylene-C substrates with hundreds of folds per centimeter. Metalizing the folded structures results in stretchable conductors with tunable properties and high conductivity. The conductors achieve extensions up to 55% strain and exhibit only a small resistance increase of a few Ohms when repeatedly stretched for more than 250 000 cycles. With the methods and design rules presented here, we access new paths for stretchable electronics based on biocompatible materials, with possible applications in biomedicine or for wearables.

## 4. Experimental Section

*$SiN_x$ Patterning*: 4-inch Si (100) wafers (525 µm thick, 10–20 Ω cm) were cleaned and gently dried with nitrogen. Afterwards, 230–240 nm of $SiN_x$ were deposited on both sides of the wafers by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. The $SiN_x$-coated wafers were then dehydration baked on a vacuum hot plate for 10 min at 250 °C, followed by treatment with hexamethyldisilazane (HMDS, Microresist Technology) primer. To this end, few drops of primer were added to a box loaded with the $SiN_x$-coated wafers and heated for 2 h at 80 °C. Then the wafers were cleaned in an acetone-water spin dryer and baked on a hot plate for 90 s at 110 °C. Photoresist (Microposit S1818 G2, Microresist Technology) was spin-coated on the wafers and patterned through UV-exposure (the shadow masks were aligned in parallel to the Si (100) crystal orientation) using a Karl Süss MA6/BA6 mask aligner and developed in Microposit MF319. After development, the photoresist was hard-baked for 60 s at 90 °C and the $SiN_x$ was patterned utilizing RIE (50 W, 150 s, $O_2$ 25 sccm; $CF_4$ 500 sccm). Remaining photoresist was then removed in the respective remover (Microposit Remover 1112A, Rohm and Haas) at 60 °C.

*Si-Mold Etching*: 1.3 L KOH-etchant (30%wt, Sigma Aldrich) saturated with isopropyl alcohol were prepared in a glass beaker and heated to 80 °C. The $SiN_x$-patterned wafers were tipped into buffered hydrogen fluoride (HF) etchant (buffered oxide etch, 5%) for 10 s to remove the native oxide and immediately after inserted into the KOH-etchant. With this setting, the etch rate for Si (100) was about 60–70 µm $h^{-1}$. All wafers were etched until complete grooves were formed. Afterwards, the wafers were rinsed thoroughly in water and the remaining $SiN_x$ was removed by etching in HF for 3 min. Additionally, the wafers were sonicated in Hellmanex III (Hellma Analytics, 2%) for 10 min to get rid of the residues.

*Surface Silanization*: The surface of the Si-molds was activated in oxygen plasma (200 W, Diener electronic GmbH) for 5 min. Each mold was enclosed in a petri dish, dispensing 70 µL of perfluorinated silane trichloro(1H,1H,2H,2H-perfluorooctyl)silane (F-OTS, Sigma Aldrich) around it. Coating of the surface occurred from the vapor phase of the silane and was completed after 1 h at room temperature. The molds were finally cleaned and sonicated in acetone for 10 min.

*Stretchable Conductors*: A 2 µm-thick parylene-C layer was deposited on the Si-molds via CVD (CVD system from Diener electronic GmbH, parylene-C dimer from TiXX Coatings GmbH). Then, a 2 nm film of Cr and a 50 nm film of Au were thermally evaporated through a stainless steel shadow mask using physical vapor deposition (PVD) in vacuum ($<2 \times 10^{-6}$ Torr, at rates of 0.3 Å $s^{-1}$ for Cr and 3 Å $s^{-1}$ for Au). The conductors were encapsulated by depositing another 2 µm-thick parylene-C layer, using an adhesion promoter (Methacryloxypropyl trimethoxysilane, A-174) in situ. The whole wafer was covered with a thin layer of PDMS (Sylgard 184, Dow Corning, 10:1 PDMS:curing-agent) and a 4-inch disk of 120 µm-thick PET foil, and cured at 40 °C for 24 h to allow peel-off of the parylene film from the Si-mold. The low curing temperatures are required to prevent the shrinking of PDMS film and the formation of wrinkles; the PET foil allows easier handling. After peel-off, an aluminum hard RIE mask was used for opening the contact pads. Thus, a 50 nm layer of Al was thermally evaporated through a steel shadow mask in a PVD chamber ($<2 \times 10^{-6}$ Torr, at rate of 8–10 Å $s^{-1}$). The encapsulating parylene-C (as well as the supporting parylene in areas neither covered by Au or Al) was removed by RIE (200 W, $O_2$ 100 sccm), patterning 10 mm × 4 mm stripes of micro-folded parylene/Au conductors with contacts. Prior to electromechanical characterization, the individual conductors were cut out with a scalpel and the exposed electrodes were covered by an Ag paste.

*Scanning Electron Microscopy (SEM)*: Measurement was performed using a Zeiss Sigma 500 field-emission SEM using an acceleration voltage of 1kV and the SE2 secondary electron detector.

*Optical Microscopy*: Freestanding stretchable conductors were stretched to 40% and fixed on rigid support prior to 3D microscopy. 3D-optical images were recorded with a Keyence digital microscope (VHX-7000, Keyence). For 2D optical microscopy, freestanding stretchable conductors were mounted in a custom-made dual-column stretcher. Images were taken at different stretch ratios.

*Electro-Mechanical Characterization*: Tensile tests were conducted with a dual column universal testing machine (Z005, Zwick Roell) equipped with a 100 N load cell and conductive pneumatic clamps. The electrical resistance of the stretchable conductors was measured between the clamps using a Keithley 2000 multimeter in 4-probe configuration. The electrical strain limit was investigated stretching at a constant speed of 10 mm $min^{-1}$ after 5 consecutive conditioning cycles with 20% strain at a speed of 20 mm $min^{-1}$. Cyclic fatigue tests were performed to 20% strain at a speed of 2 mm $s^{-1}$, with 10 preceding cycles at a speed of 20 mm $min^{-1}$ every 2000 cycles to get a high-resolution strain response. The interval between slower cycles was extended for fatigue tests with $250 \times 10^3$ cycles.

*Finite Element Analysis*: The commercial software package COMSOL Multiphysics was used to predict the mechanical response of the stretchable conductors. The Young's modulus and Poisson's ratio of gold were 80 GPa and 0.415 while those of parylene-C were 3.2 GPa and 0.4. The thickness of the parylene-C layers was 2 µm (for each substrate and encapsulation) and the metal layer was 50 nm thick. The dimensions of the sample were $g = 100$, $c = 100$, with a shape as depicted in Figure S3, Supporting Information. In the simulation, a 2D plane strain model was used to simulate the deformation of the stretchable conductor that the width of the model was considered to be infinite. A representative unit of the stretchable conductor was analyzed and used a periodic boundary condition along the stretching direction. The mesh density was high enough to ensure accuracy. The strain was applied by prescribing the displacement of the edges of the stretchable conductor.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Author Contributions

E.D.G. and V.Đ. conceived the research project; F.H., V.Đ., and E.D.G. designed the research; F.H., M.J., and M.N. did the fabrication; F.H. conducted the electro-mechanical characterization; M.J., E.D.G., and F.H. recorded the microscopy images; G.M. performed FE analysis; F.H. and M.K. analyzed the data; F.H. wrote the manuscript with contributions from all authors; E.D.G., V.Đ., and M.K. supervised the research.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

microfabrication, origami, parylene, stretchable electronics

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